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DOCUMENT-IDENTIFIER: US 6362763 B1
TITLE: Method and apparatus for oscillation recovery in a delta-sigma A/D converter

Abstract Text (1):
A method and apparatus for recovering from an unstable oscillating condition in a delta-sigma A/D converter modulator circuit. A modulator circuit is disclosed having integrator stages, each having a first switch across the input terminals of the integrator stage and a second switch across the output terminals of the integrator stage. In another embodiment of the invention, the integrator stage comprises a differentially structured operational amplifier having a first restore switch coupled across the input terminals, a second restore switch across the output terminals, and four disconnect switches, one each coupled between the operational amplifier inputs and ends of the first restore switch and between the operational amplifier outputs and ends of the second restore switch. In operation, an unstable condition detector monitors an output of the A/D modulator circuit and generates a restore signal to the integrator stages upon detection of an unstable condition. Upon receipt of the restore signal, each of the restore switches closes and each of the disconnect switches opens to effectively isolate integrating capacitors for each of the integrator stages from the operational amplifiers of the respective integrator stages.

Brief Summary Text (3):
The present invention relates generally to a delta-sigma modulator for use with an analog-to-digital converter. More particularly, the present invention relates to the use of a delta-sigma modulator with circuitry to detect instabilities in the modulator and to restore the modulator to a stable operating condition.

Brief Summary Text (6):
One well-known type of oversampling A/D conversion technique uses a modulator commonly referred to as a delta-sigma modulator. In an A/D converter using a delta-sigma modulator including integrator(s), comparator(s) and a digital-to-analog converter ("DAC") in the feedback path, a low-pass decimation filter is used following the modulator to provide necessary filtering. The analog input is modulated to a digital bit stream, typically several bits wide.

Brief Summary Text (7):
As shown in the block diagram of FIG. 1, a delta-sigma modulator 2 receives an input 4 and produces an output 6. A delta-sigma modulator 2 may include one or more integration stages 8 and 10. Feedforward paths a1 and a2 are provided from the outputs of each integration stage 8 and 10 to a first summing junction 12 on the non-inverting input to a comparator 14. A feedback path 15 includes a DAC b and extends between the output 6 and a second summing junction 16.

Brief Summary Text (8):
Typically, it is desirable in the design of a delta-sigma modulator to reduce quantization noise. Reduction of quantization noise may be achieved by the selection of a transfer function for the overall modulator that possesses high in-band gain and high out-of-band attenuation, thereby shaping the quantization noise spectrum advantageously. To appropriately shape the overall modulator transfer function, one or more additional integration stages are included within the modulator circuitry, thereby increasing the order of the modulator.

Brief Summary Text (10):
One approach to correcting the instability found in higher order modulators (three or more integration stages) is to use state-variable clamping techniques. FIG. 2

shows an integration stage 18 of a modulator including an op-amp 20 having an integration capacitor 22 and a limiter 24 coupled between the non-inverting input and the output of the op-amp 20. A non-linear element, such as a limiter, coupled across the integrating capacitor 22 prevents large values from appearing at the integrator output. Typically, for a higher order modulator circuit, the non-linear elements are set to turn "ON" at about 20-50% higher than the peak-to-peak integrator swings. One example of a limiting scheme implemented in an integrator stage is shown in U.S. Pat. No. 5,977,895 to Murota et al. (Nov. 2, 1999), entitled "WAVEFORM SHAPING CIRCUIT FOR FUNCTION CIRCUIT AND HIGH ORDER DELTA SIGMA MODULATOR." For the approach shown in Murota et al., however, the input signal at each stage must be limited to a few hundred millivolts to maintain stability. As a result, the first stage integrator capacitor tends to be very large relative to the input capacitor. In a high performance A/D modulator design where input capacitors are relatively large, the addition of an even larger first stage integration capacitor results in an area- and power-intensive circuit.

Brief Summary Text (13):
U.S. Pat. No. 5,012,244 to Wellard et al. (Apr. 30, 1991), entitled "DELTA-SIGMA MODULATOR WITH OSCILLATION DETECT AND RESET CIRCUIT," includes an example of the first method of sensing instability for higher order modulators. FIG. 3, herein, is similar to that shown in FIG. 1 of the Wellard et al. patent and shows a circuit in which a fourth order delta-sigma modulator 30 uses an oscillation detect comparator 32 to detect instability in the signal at the output of the second integrator 36. If instability is detected, the oscillation detect comparator 32 resets the circuit by short-circuiting the outputs of each of the four integrators 34, 36, 38 and 40 with its respective input by closing a switch 42, 44, 46 and 48 coupled across each of the integrators 34, 36, 38 and 40.

Brief Summary Text (14):
FIG. 4 includes a more detailed diagram of a single integrator stage 50 of the prior art delta-sigma modulator circuit of FIG. 3. Each stage 50 includes an integrating capacitor 52 and a switch 54 coupled in parallel between the output 56 and an input 58 of an op-amp 60. The op-amp 60 shown in FIG. 4 is configured as a single-ended structure, meaning it has only a single output, rather than as a differential-ended structure, meaning it has two outputs. Both singular and differential structures for op-amps are well known in the art.

Brief Summary Text (19):
It is another object of the invention to have a high order delta-sigma modulator circuit which is capable of retaining stored common mode information throughout a restore operation.

Drawing Description Text (3):
FIG. 1 is a diagram of a prior art delta-sigma modulator circuit for an A/D converter;

Drawing Description Text (4):
FIG. 2 is a diagram of a prior art integrator stage for a delta-sigma modulator having a voltage limiter coupled across an input and output;

Drawing Description Text (5):
FIG. 3 is a diagram of a prior art implementation of a delta-sigma modulator;

Drawing Description Text (6):
FIG. 4 is a diagram of a prior art integrator stage for the delta-sigma modulator of FIG. 3;

Drawing Description Text (7):
FIG. 5 is a diagram illustrating an integrator stage for a delta-sigma modulator according to a first embodiment of the present invention;

Drawing Description Text (8):
FIG. 6 is a diagram illustrating an integrator stage for a delta-sigma modulator according to a second embodiment of the present invention;

Drawing Description Text (9):
FIG. 7 is diagram of a delta-sigma modulator circuit for an A/D converter comprising a plurality of integrator stages according to embodiments of the present invention;

Drawing Description Text (10):
FIG. 8 is another diagram of a delta-sigma modulator circuit for an A/D converter comprising a plurality of integrator stages according to embodiments of the present invention and having different layout than the delta-sigma modulator circuit shown in FIG. 7; and

Detailed Description Text (2):
FIG. 5 illustrates an integrator stage, without the input switched-capacitor branch, for a delta-sigma modulator of an A/D converter circuit according to a first embodiment of the present invention. The integrator stage 62 of FIG. 5 comprises a differentially structured op-amp 64 having inverting and non-inverting inputs, and inverting and non-inverting outputs. Similar to other known integrator stages, the integrator stage 62 comprises a first integrating capacitor 66 coupled between the inverting input and the non-inverting output, and a second integrating capacitor 68 coupled between the non-inverting input and the inverting output. Distinct from known integrator stages, however, the integrator stage of this first embodiment includes a first restore switch 70 coupled between the inverting and non-inverting inputs, and a second restore switch 72 coupled between the inverting and non-inverting outputs. In operation, when the integrator stage 62 receives a restore signal, the first and second restore switches 70 and 72 are activated to a closed state to place the integrator stage in a stable, known state. Because the restore switches 70 and 72 are coupled, respectively, between the inputs and the outputs rather than across each of the integrating capacitors 66 and 68, rather than eliminating the common mode voltage across the integrating capacitors 66 and 68, the charge corresponding to the common mode voltage is redistributed between the integrating capacitors 66 and 68 to remove the differential voltage between the inputs and between the outputs of the op-amp 64.

Detailed Description Text (3):
For conventional delta-sigma modulator circuits, such as that disclosed by Wellard, et al. (U.S. Pat. No. 5,012,244), upon completion of a reset operation, the common mode voltage of the input stage is the same as the common mode voltage of the output stage. However, for some op-amp topologies, the input common mode voltage of the op-amp is required to be different than the output common mode voltage for the op-amp to operate properly. When the input and output common mode voltages are the same, it may take a number of cycles of operation for the input common mode voltage to attain a necessary level for normal operation. Contrarily, with the embodiments of the present invention disclosed herein, the oscillation recovery is completed immediately upon completion of the restore operation without disturbing the input common mode voltage. In this way, the delta-sigma modulator circuit will return to normal operation immediately upon completion of the restore operation.

Detailed Description Text (4):
For certain op-amp topologies, in addition to the restore switches respectively coupled across the inputs and outputs of the op-amp, disconnect switches to isolate the inputs and outputs of the op-amp from surrounding circuitry are preferable. FIG. 6 illustrates a second embodiment of an integrator stage for a delta-sigma modulator of an A/D converter circuit. In addition to the elements of the integrator stage shown in FIG. 5, the integrator stage 74 shown in FIG. 6 includes four disconnect switches 76, 78, 80 and 82 which open when the integrator stage 74 receives a restore signal. By activating the disconnect switches 76, 78, 80 and 82 to an open state and activating the restore switches 70 and 72 to a closed state during a restore operation, the op-amp 64 is isolated from surrounding circuitry. If the op-amp 64 is not isolated from surrounding circuitry during a restore operation, large current amounts may flow through the outputs of the op-amp 64 due to offset. Because the excess current flow through the op-amp outputs results in unnecessary power consumption, by isolating the op-amp 64, power is preserved. This configuration is particularly advantageous for class AB op-amps which are capable of much larger output currents in relation to input currents than class A op-amps which have fixed output currents regardless of the input current.

Detailed Description Text (5):
FIG. 7 includes a circuit diagram of a delta-sigma modulator circuit 84 for use in an A/D converter circuit. The modulator circuit 84 comprises an input conductor 86, an output conductor 88, a plurality of integrator stages 90, 92 and 94 coupled in series, and a feedforward conductor a.sub.1, a.sub.2 and a.sub.n coupled to the output of each integrator stage 90, 92 and 94. The feedforward conductors a.sub.1, a.sub.2 and a.sub.n are each coupled to a first summing junction 96, the output of which is coupled to the input of a quantizer 98. In place of a quantizer 98, any device which generates a digital output in response to an analog input would suffice, such as, but not limited to, a comparator, a 1-bit A/D converter, and the like. The output of the quantizer 98 is coupled to the output conductor 88. The output conductor 88 is coupled to a feedback conductor 100 which is also coupled through a DAC 101 to a second summing junction 102 with the input conductor 86. The output of the second summing junction 102 is coupled to the input of the first integrator stage 90.

Detailed Description Text (6):
Instability detector and restore circuitry is also included in the modulator circuit for monitoring the operating characteristics of the modulator to determine if the modulator is operating at or near an unstable condition. When it is determined that the modulator is at or near an unstable condition, a restore signal is generated to selectively restore particular integrator stages. The criteria for determining an unstable condition may be embodied as fixed threshold values, or variable threshold values, or combinations of values such as an input level beyond a threshold for a number of cycles. For the embodiment shown in FIG. 7, the output conductor 88 is also coupled to the input of a 4-bit counter 104, including necessary logic circuitry for monitoring consecutive "1s" and "0s" on the output conductor 88. The output of the 4-bit counter 104 is coupled to each of the integrator stages 90, 92 and 94 for selectively restoring the integrator stages 90, 92 and 94 to stable conditions. It will be clear to one of ordinary skill in the art that the operating characteristics of the modulator may be monitored at any point within the modulator circuit such as at the input, at the output, or at the input or output of any integrator stage. FIG. 8 illustrates an embodiment wherein circuitry 110 for detecting instability and generating a restore signal is coupled near the input 86 rather than to the output 88.

Other Reference Publication (1):
"Delta-Sigma Data Converters--Theory, Design, and Simulation" edited by Steven R. Norsworthy, Richard Schreier and Gabor C. Temes, IEEE Press pp. 183-185, p. 190.

CLAIMS:

4. The analog-to-digital converter modulator circuit of claim 1, wherein the modulator circuit is configured as a delta-sigma modulator circuit.

7. A method for operating a delta-sigma modulator circuit, the method comprising: monitoring an output of the modulator circuit for instability; and activating a first restore switch across inputs and a second restore switch across outputs of at least one integrator stage in response to detecting instability.

18. The analog-to-digital converter modulator circuit of claim 14, wherein the modulator circuit is configured as a delta-sigma modulator circuit.